

Application/Control Number: 10/016,939

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COMPLETE LISTING OF CLAIMS

1. (Original) A chip stack comprising:

a flex circuit comprising:

a flex substrate;

a first conductive pattern disposed on the flex substrate; and

a plurality of leads extending from the flex substrate and electrically

connected to the first conductive pattern;

at least two integrated circuit chip packages electrically connected to the

first conductive pattern.

2. (Original) The chip stack of Claim 1 wherein:

the flex substrate defines opposed top and bottom surfaces; and

the first conductive pattern comprises:

a first set of flex pads disposed on the top surface of the flex substrate;

and

a second set of flex pads disposed on the bottom surface of the flex substrate;

the flex pads of the first and second sets being electrically connected to the leads, with one of the integrated circuit chip packages being disposed upon the top surface of the flex substrate and electrically connected to at least some of the flex pads of the first set and one of the integrated circuit chips being

disposed upon the bottom surface of the flex substrate and electrically connected to at least some of the flex pads of the second set.

3. (Original) The chip stack of Claim 2 wherein the flex pads of the first and second sets are arranged in identical patterns.

4. (Original) The chip stack of Claim 2 wherein:

the flex substrate has a generally rectangular configuration defining opposed pairs of longitudinal and lateral peripheral edge segments; and

the leads extend from at least one of the longitudinal and lateral peripheral edge segments of the flex substrate.

5. (Original) The chip stack of Claim 1 wherein each of the leads is an S-lead.

6. (Original) The chip stack of Claim 2 wherein the integrated circuit chip packages each comprise:

a package body having opposed, generally planar top and bottom surfaces; and

a plurality of conductive contacts disposed on the bottom surface of the package body;

the conductive contacts of one of the integrated circuit chip packages being electrically connected to respective ones of the flex pads of the first set, with the conductive contacts of one of the integrated circuit chip packages being electrically connected to respective ones of the flex pads of the second set.

7. (Original) The chip stack of Claim 6 wherein the flex pads of the first and second sets and the conductive contacts are arranged in identical patterns.

8. (Original) The chip stack of Claim 6 wherein each of the integrated circuit chip packages comprises a CSP device.

9. (Original) The chip stack of Claim 8 wherein the integrated circuit chip packages are each selected from the group consisting of:

a BGA device;

a fine pitch BGA device; and

a flip chip device